REMARKS

The Examiner's Action mailed on October 8, 2002 has been received and its contents carefully considered. Additionally attached to this Amendment is a Request for Continued Examination (RCE), thus ensuring the entry of this Amendment.

In this Amendment, independent claims 1, 4, 5 and 7 have been amended. Claims 1, 4, 5 and 7 are the only independent claims pending in the application. Claims 1-10 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 1, 4 and 8 as being obvious over *Lin* (USP 6,184,580) in view of *Dibble et al.* (USP 6,040,631). It is submitted that these claims are patentably distinguishable over the cited combination of references for at least the following reasons.

Applicant's independent claim 1 is directed to a semiconductor device which includes, *inter alia*, a heat spreader having a flat principal surface and having a semiconductor chip and a wiring board provided over the flat principal surface. A common adhesive layer is provided over the principal surface of the heat spreader and bonds both the semiconductor chip and the wiring board to the heat spreader. As such, a heat transfer effect between the semiconductor chip and the heat spreader is about equal to a heat transfer effect between the wiring board and the heat spreader. As such, this claimed configuration reduces any adverse effects which may be caused by uneven heat transferring, such as warping or inadvertent separation of the various components from the heat spreader. This claimed device is not disclosed or suggested by the cited references.

Lin discloses a ball grid array package having a silicon chip 20 adhered to a heat spreader 26 using a first adhesive layer 24. This reference also discloses attaching conductive leads 36 to the surface of the heat spreader 26 using a second adhesive layer 38. Thus, this reference does not disclose or otherwise suggest attaching a semiconductor chip and wiring board to a heat spreader using a common adhesive layer, as recited in claim 1. As a result, the configuration shown by *Lin* will likely be subjected to uneven heat transfer effects, which problem is rectified utilizing Applicant's claimed invention.

The Examiner's Action also relies on the teachings of *Dibble et al.* *Dibble et al.* disclose a method of an improved cavity ball grid array circuit package, in which a chip 14 is attached to a heat spreader 12 using both a first adhesive 16 and a second adhesive 18. This reference further discloses providing a chip carrier 26 which is presumably attached to the heat spreader 12 utilizing the first adhesive 16, as shown in Figure 2. This reference discloses that it is important that two separate adhesives be used, so as to provide allegedly greater flexibility, as discussed in column 4, lines 57-64. Thus, not only does this references not disclose or otherwise suggest a wiring board and a semiconductor chip both being attached to a heat spreader utilizing a common adhesive layer, as recited in claim 1, but this reference specifically teaches away from such a configuration, since such a configuration would presumably, by the teachings of this reference, result in less flexibility, which is adverse to the goals being sought by this reference. As such, it is submitted that Applicant's independent claim 1 is *prima facie* patentably distinguishable over this combination of references, and it is requested that this claim be allowed.

Applicant's independent claim 4 is directed to a method of manufacturing a semiconductor device, which recites similar features to those found within allowable independent claim 1. It is submitted that claim 4 is patentably distinguishable over the cited references for reasons similar to those given above with respect to independent claim 1. It is likewise submitted that this claim is patentably distinguishable over the cited references.

Further, dependent claim 8 is submitted to be patentably distinguishable over the cited references for at least the same reasons as independent claim 1, from which this claim depends, as well as for the additional features recited therein. It is requested that this claim be allowed, and it is further requested that these rejections be withdrawn.

The Examiner has further rejected claims 2 and 3 as being obvious over *Lin*, and further in view of *Yamagata et al.* (USP 5,828,127). As noted above, Applicant's independent claim 1 is *prima facie* patentably distinguishable over *Lin*. Moreover, *Yamagata et al.* only discloses providing a fin 19 which is attached utilizing an adhesive 20. This reference does not overcome the above-noted deficiencies of *Lin*, so that the resulting combination does not disclose or otherwise suggest the features recited within independent claim 1. As such, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein. It is requested that these claims be allowed and it is further requested that these rejections be withdrawn.

The Examiner has rejected claims 5-7, 9 and 10 as being obvious over *Lin* in view of *Yamagata*, and further in view of *Moscicki* (USP 6,064,115) and *Shin* (USP

5,807,769). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Applicant's independent claim 5 is directed to a method of manufacturing a semiconductor device. The method includes forming a wiring board over a first adhesive layer. The wiring board has a through opening. A semiconductor chip is formed over a second adhesive layer and is disposed in the through opening so that all side surfaces of the semiconductor chip are completely surrounded by the wiring board. Applicant's claimed invention also recites that the second adhesive layer and part of the semiconductor chip are sealed with an encapsulating resin. In accordance with claim 5, metal thin wires and the semiconductor chip are then sealed with a second encapsulating resin after the first encapsulating resin has been cured. Claim 7 differs from claim 5 in that after the encapsulating resin has at least partially cured, the metal thin wires and the semiconductor chip are sealed with more of the encapsulating resin. In accordance with both of these claims, two separate resin sealing steps are performed. The advantages of these methods are discussed in Applicant's specification. These claimed methods are neither disclosed nor suggested by the cited references.

The only reference relied upon by the Examiner that discloses utilizing two resin operations is *Shin*. This references discloses providing leads 4 around a chip 2, and using a first encapsulating part 6, 6a and a second encapsulating part 7a, 7b, to seal the chip 2 and the leads 4. However, as is clear from the specification of this reference, the leads 4 do not completely surround all of the side surfaces of the semiconductor chip, as recited in claims 5 and 7. That is, the leads 4 are spaced apart from one

another, so that there are spaces between the leads. As such, it is submitted that claims 5 and 7 are *prima facie* patentably distinguishable over the combination relied upon by the Examiner, and it is requested that these claims, and the claims dependent therefrom, be allowed. It is further requested that these rejections be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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RHB:crh

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice Amended) A semiconductor device, comprising:

a semiconductor chip;

metal thin wires respectively connected to electrodes on said semiconductor chip;

a wiring board having an opening for accommodating said semiconductor chip and being electrically connected to said semiconductor chip by said metal thin wires;

a heat spreader having a flat principle surface, and having said semiconductor chip and said wiring board provided over the flat principal surface [thereon];

[an] a common adhesive layer which is provided over [a principle] the principal surface of said heat spreader and bonds both said semiconductor chip and said wiring board to said heat spreader, [each other] so that a heat transfer effect between said semiconductor chip and said heat spreader is about equal to a heat transfer effect between said wiring board and said heat spreader;

and

an encapsulating resin for sealing at least said metal thin wires,

wherein said semiconductor chip is disposed in the opening of said wiring board, and is separated from edges of said wiring board that collectively define the opening by a space so that said semiconductor chip does not completely cover said heat spreader within the opening, and

wherein a portion of said heat spreader within the opening that is not covered by said semiconductor chip being completely covered by said adhesive layer.

4. (Twice Amended) A method of manufacturing a semiconductor device, comprising the following steps:

preparing a heat spreader having a flat, principle surface;

forming [an] a common adhesive layer over [a] the principal surface of said heat spreader;

disposing a semiconductor chip and a wiring board over said common adhesive layer, the wiring board having an opening for accommodating said semiconductor chip, said semiconductor chip being disposed in the opening of said wiring board, and being separated from edges of said wiring board that collectively define the opening by a space so that said semiconductor chip does not completely cover said heat spreader within the opening, a portion of said heat spreader within the opening that is not covered by said semiconductor chip being completely covered by said common adhesive layer;

connecting electrodes of said semiconductor chip and said wiring board by metal thin wires; and

sealing at least said metal thin wires with an encapsulating resin,

wherein the common adhesive layer is utilized to bond both the semiconductor chip and the wiring board to the principal surface of the heat spreader, so that a heat transfer effect between the semiconductor chip and the heat spreader is about equal to a heat transfer effect between the wiring board and the heat spreader.

5. (Twice Amended) A method of manufacturing a semiconductor device, comprising the following steps:

preparing a heat spreader;

forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;

forming a wiring board over said first adhesive layer, the wiring board having a through opening;

forming a semiconductor chip over said second adhesive layer and disposing the semiconductor chip in the through opening so that all side surfaces of said semiconductor chip are completely surrounded by said wiring board;

connecting electrodes of said semiconductor chip and said wiring board by metal thin wires;

sealing said second adhesive layer and part of said semiconductor chip with a first encapsulating resin; and

sealing said metal thin wires and said semiconductor chip with a second encapsulating resin after said first encapsulating resin has been cured.

7. (Twice Amended) A method a manufacturing a semiconductor device, comprising the following steps:

preparing a heat spreader;

forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;

forming a wiring board over said first adhesive layer, the wiring board having a through opening;

forming a semiconductor chip over said second adhesive layer and disposing the semiconductor chip in the through opening so that all side surfaces of said semiconductor chip are completely surrounded by said wiring board;

connecting electrodes of said semiconductor chip and said wciring board by metal thin wires;

sealing said second adhesive layer and part of said semiconductor chip with an encapsulating resin; and

after said encapsulating resin has at least partially cured, sealing said metal thin wires and said semiconductor chip with more of said encapsulating resin.